SAUSVF: SVF player for SAU510-USB Iso Plus Emulator

Features:

- Program FPGA, CPLD, configur FPGA which is in the TI DSP JTAG circuit
- Supports enhancements (LOOP/ENDLOOP) from Lattice Semiconductor
- Simple command line utility. Can be used in batch-files, connected to various development environments as external tool.
- All emulator operating modes are controlled through command line
- Allows to connect several emulators to one PC

SVF player is designed for boundary scan tasks that are set through specification "Serial Vector Format Specification Rev.E". Most FPGA software development environments permit to generate SVF output file. Thus you can configure and program FPGA and CPLD through SAU510-USB Iso Plus Emulator.

Command line for the SVF-player:

sausvf svf_file_name [-option1 [-option2] …]

svf_file_name – path to SVF file.

Operations:

-SN <S/N>	Use an emulator with a specified serial number
-NT -notckr	Disable return clock signal usage (TCKR, RTCK, TCK_RET). Used when the target does not generate this signal. In this mode the emulator generates internal signal, that is similar to the return clock signal itself. The emulator does not use TCKR input.
-A -adaptive	Enable adaptive clocking mode. In this mode the next rising edge is generated not earlier than the previous edge returns through return clock signal circuit. The parameter that defines TCK frequency defines the maximum allowed TCK frequency. Adaptive clocking mode can not be used without return clock signal.
-F <freq> -frequency <freq>	Sets TCK frequency or maximum allowed TCK frequency in the adaptive clocking mode. If you use this parameter, the frequency is set forcibly and the SVF-file instructions for frequency setting are ignored. If you do not use this parameter the frequency is set by SVF instructions. The frequency is specified in Hz, e.g. 1000000 or 1E6 equal 1 MHz.
-NR -noterminators	Disables impedance matching circuits from TDO and TCKR emulator inputs. Parallel matching 120 ohm to half target power voltage is enabled on default.
-CLKD <delay>	Additional delay TCK->TCKR for the mode without return clock signal. Additional delay is zero by default. It approximately equals TCK and TCKR connecting at the target jack. The delay is set by intervals from 0 to 3 of 4,8 ns each.

-E -fallingedge	Generating TMS and TDO from the falling edge of the return clock signal. It corresponds to IEEE1149.1, but the maximum TCK frequency in this case is lower than the default TCK frequency in the mode when TMS and TDO are generated from the rising edge of TCK.
-TMSD <delay> -TDOD <delay>	Additional TMS and TDO delay relative to TCKR edge. It is used for tweaking emulator when operating at the clock frequencies above 20 MHz (for more information see User's Guide SAU510-USB ISO PLUS Emulator). The delay is set by intervals from 0 to 7 of 4,8 ns each.
-L <delay> -linkdly <delay>	JTAG circuit delay. The number of additional trigger-synchronizers for TMS, TDO and TDI circuits which are inside and outside the emulator. There are 3 trigger-synchronizers in the emulator. That is why the parameter is 3 on default. If you use any additional synchronizer in the target or if you use the emulator at higher than 20 MHz frequencies (e.g. clock signal cycle is shorter than signal propagation through emulator galvanic isolation) you can change this parameter. The delay is set in TCKR cycles. The allowed values are 3..31. For more information see User's Guide SAU510-USB ISO PLUS Emulator.
-E0 <value> -emu0 <value> -E1 <value> -emu1 <value>	Sets EMU0 and EMU1 pins status during SVF player operating. <value> can be 0 or 1. It allows to turn TI DSPs to various scan modes, including emulation-debug and boundary scan modes. On start after setting the defined values at these pins, the emulator generates an impulse at TRST to change JTAG-controller's mode.